Department of Mathematics and Computer Science

Thursday, October 6, 2022, 4:00 pm

COLLOQUIUM TALK

Speaker: Kun-Chih (Jimmy) Chen (National Sun Yat-sen University)

Old Main 2231

Deep Neural Network on Chip (DNNoC) Design Paradigm for Future AI Accelerator Realization

Abstract:

Deep Neural Networks (DNN) have shown significant advantages in many domains. The contemporary DNN comprises tens to thousands of layers, making DNN operations become computation and communication intensive. General-purpose processors cannot efficiently handle this massive amount of data in an acceptable time. To tackle this issue, the design of DNN accelerators has received much attention from academia and industry in recent years. However, the intensive communication among neurons in different layers leads to complicated interconnection patterns that lack flexibility and scalability while suffering from extensive memory accesses. In this talk, I will introduce a novel design paradigm using Network-on-Chip (NoC) interconnection to implement Deep Neural Network on Chip (DNNoC). According to the different design perspectives, I propose three different DNNoC designs: 1) Homogeneous DNNoC design, 2) Heterogeneous DNNoC design, and 3) Reconfigurable DNNoC design, which leverage the DNN accelerator design in the future. Besides, the algorithms and architecture optimizations for each DNNoC design paradigm will also be introduced in this talk.

Bio:

Kun-Chih (Jimmy) Chen received his PhD degree from Nation Taiwan University, Taiwan (NTU), in Graduate Institute of Electronics Engineering (GIEE) in 2013. He is currently an Associate Professor in the Computer Science and Engineering Department of National Sun Yat-sen University (NSYSU). Since 2020, Dr. Chen has been nominated as a Distinguished Young Scholar of NSYSU. His research interests include Multiprocessor SoC (MPSoC) design, Neural network learning algorithm design, Reliable system design, and VLSI/CAD design. Dr. Chen received the Best Paper Award of VLSI-DAT'14, Best Paper Award of IJCC'16, Best PhD Dissertation Award of IEEE Taipei Section, Taiwan Comprehensive University System (TCUS) Young Scholar Innovation Distinction Award, Best Student Paper Award of IEEE ISCAS'20, IEEE Tainan Section Best Young Professional Member Award, Exploration Research Award of Pan Wen Yuan Foundation, Taiwan IC Design (TICD) Society

Outstanding Young Scholar Award, and Chinese Institute of Electrical Engineering (CIEE) Outstanding Youth Electrical Engineer Award. Dr. Chen is the referee of many IEEE journals and conferences, including TC, TPDS, TCAS-I, TVLSI, TCAD, ISCAS, ICASSP, VLSI-DAT, etc. Dr. Chen has served as the Guest Editor of the Journal of Systems Architecture (JSA), Nano Communication Network (NanoComNet), and IEEE Journal on Emerging and Selected Topics in Circuits and Systems (JETCAS). Besides, he served as a Technical Program Committee (TPC) chair of the International Workshop on Network on Chip Architectures (NoCArc) in 2018 and the General Chair of the same workshop in 2019. He is an IEEE senior member, ACM member, APSIPA member, Chinese Institute of Electrical Engineering (CIEE) life member, and life member of the Taiwan IC Design (TICD) Society.

RECEPTION IN FACULTY LOUNGE AT 3:30 PM.
EVERYONE WELCOME (EVEN IF YOU ARE UNABLE TO ATTEND THE TALK)